

CDF Run II B Silicon Upgrade

PAC Meeting

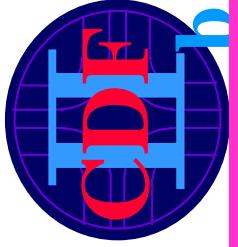
November 2nd, 2001

Brenna Flaugher

Run II B Silicon Project Co -leader

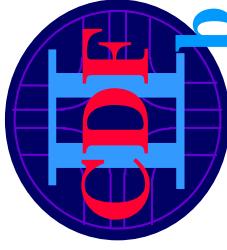
Fermilab

For the CDF Collaboration



CDFRunIIIB Silicon Upgrade: Outline

- Design goals and Constraints
 - Layout: sensors, hybrids, staves
 - Material: comparison to RunIIA
 - DAQ: new components
 - Tracking Layout studies
 - Cost and Schedule
 - Conclusions
-
- Note: Additional mechanical and simulation studies may result in some changes in the layout, but these changes will be motivated by simplification and will not increase the scope of the project.



RunIIB

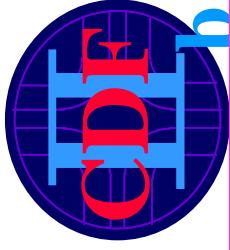
Lab plan stored through 2007, majority of Lum. after 2004!

Year	# months	L_{cum} (fb^{-1})	L ($\text{cm}^{-2}\text{s}^{-1}$)	Comment
2001	8	0.2	$3 \cdot 10^{31}$	
2002	10	1	$8 \cdot 10^{31}$	
2003	8	2.0	$1.2 \cdot 10^{32}$	go to 132 ns
2004	11	3.8	$2 \cdot 10^{32}$	NuMI starts operating
2005	8	6.3	$4 \cdot 10^{32}$	
2006	11	10.7	$5 \cdot 10^{32}$	
2007	10	14.7	$5 \cdot 10^{32}$	

RunIIB working group found that L00 and SVXII will not survive:

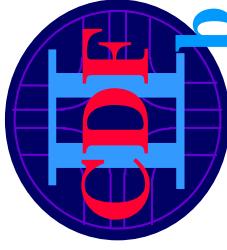
CDF	R_{\min} (cm)	L (fb^{-1})
L00	1.35	7.4
L0	2.54	4.3
L1	4.12	8.5
L2	6.52	10.7
ISL	20 - 28	>40
DOIMs	14	5.7

- Run2b Working Group report used Run1 and Run1b data to estimate lifetime of Run2a detector.
- Run2a is instrumented with TLDs
- Preliminary results (Oct. 30th!) confirm WGA assumptions on radial dependence of dose
- Studies and analysis of TLD data will continue, more data is needed

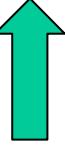


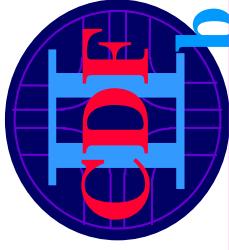
Silicon Upgrade for Run IIIB

- Goal: Ready for installation by June 2004!
- Short turnaround (~6m) between Run IIA and IIIB
 - Only viable option is complete replacement
- Design Goals:
 - Robust, simple and reliable design
 - Minimize the cost
 - Match or exceed performance of Run IIA silicon detector
 - Minimize changes to infrastructure: DAQ or cooling systems
- Big changes since April design: Use fine pitch signal cables only on L0! Hybrids are glued to Sensors on layers 1 - 6
- Continue to pursue common solutions with D0 through task force meetings: chip, sensor specs, beam pipe, ...



Radiation Tolerance Implications

- SVXII double-sided silicon limited in bias voltage
 - Ø Needs single-sided, high voltage silicon detectors (L00style)
 - Ø To retain tracking capability we need at least twice as many detectors:
 **Moresilicon**
 - Ø To survive high radiation doses we need to operate the silicon at a lower temperature
 - Sensors must be actively cooled
- The current SVX3 chip (Honeywell 0.8um) cannot survive
 - Ø The SVX4 chip is being designed. Uses naturally 0.25um standard technology



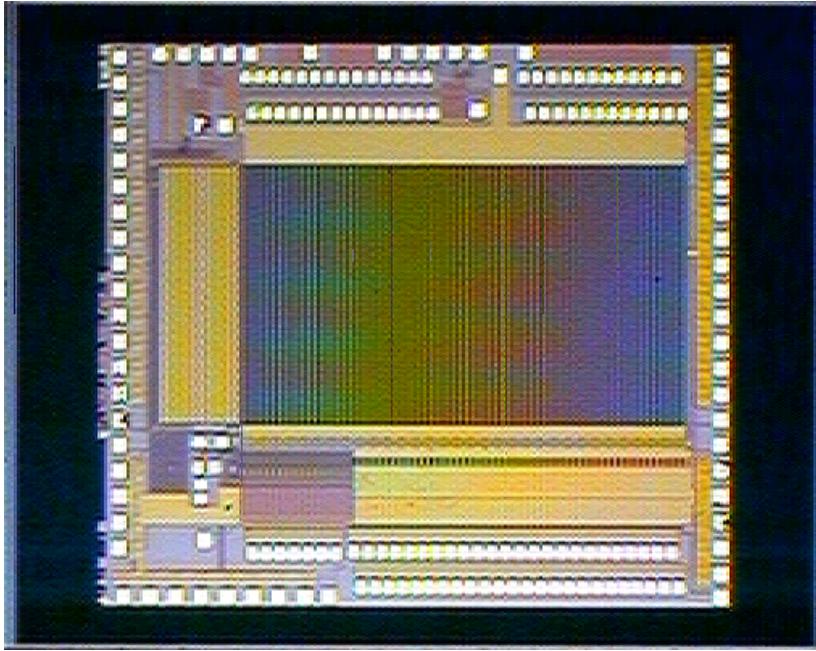
SVX4Chip

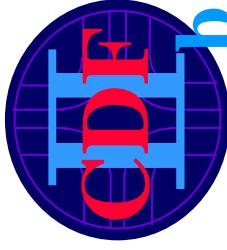
Great progress since last PAC Meeting

- ⌚ Test chip came back in early August – entire frontend (preamplifier+pipeline) functions!
- ⌚ Chips irradiated to 16 Mrad with Co -60 facility, no changes observed – T. Zimmerman
“If some of the other components on the board hadn’t melted, I wouldn’t have believed it was irradiated.”
- ⌚ S/N 30% better than SVX3
- ⌚ CDF and D0 will use same chip

October 22 SVX4 chip preview found:

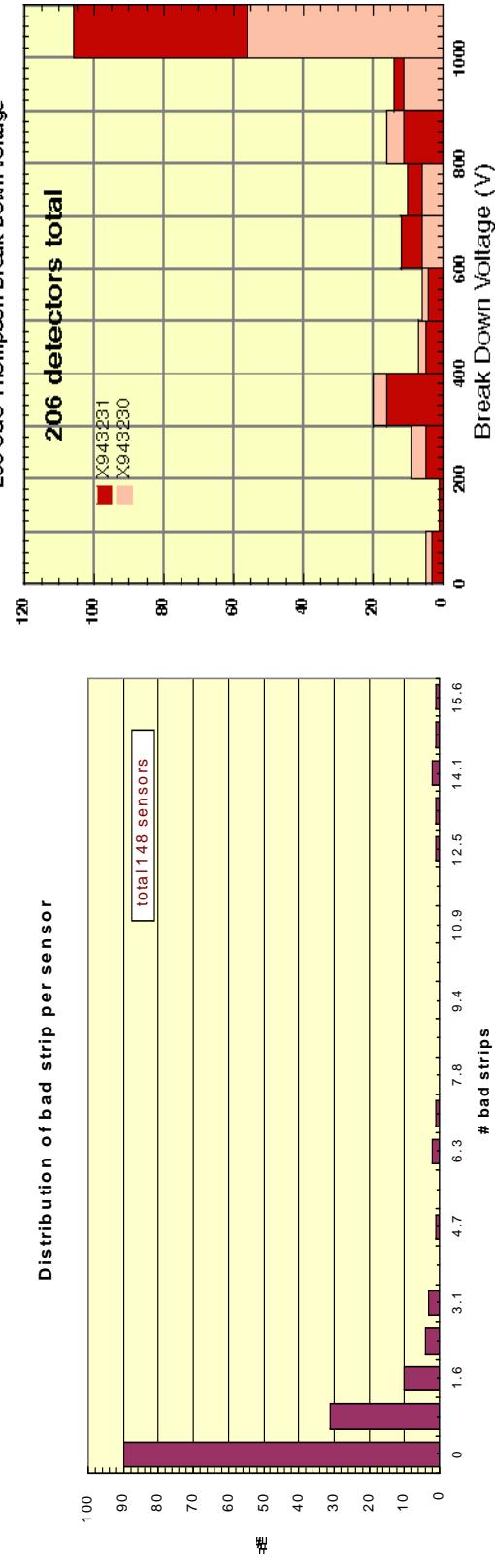
- ⌚ Project is in reasonably good shape
- ⌚ full chip submission delayed by a few weeks (not months).
- ⌚ Expect chips back in early 2002 since turn around is only 6 -8 weeks.

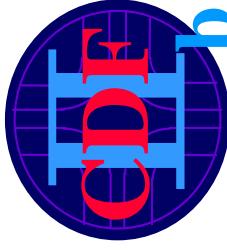




Silicon Sensors

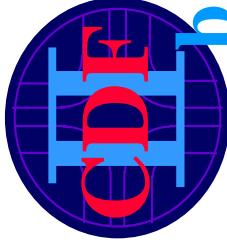
- All detectors are single-sided and based on the high voltage geode (CMS, ATLAS, L00)
 - Easy to build, test and handle
 - No R&D necessary (except for testing 900 gr thin silicon)
 - High yield and minimum number of problematic channels per detector ($< 1\%$ in most of the detectors)
 - Mask Design nearing completion – first orders this fall
- Experience with L00 Sensors:





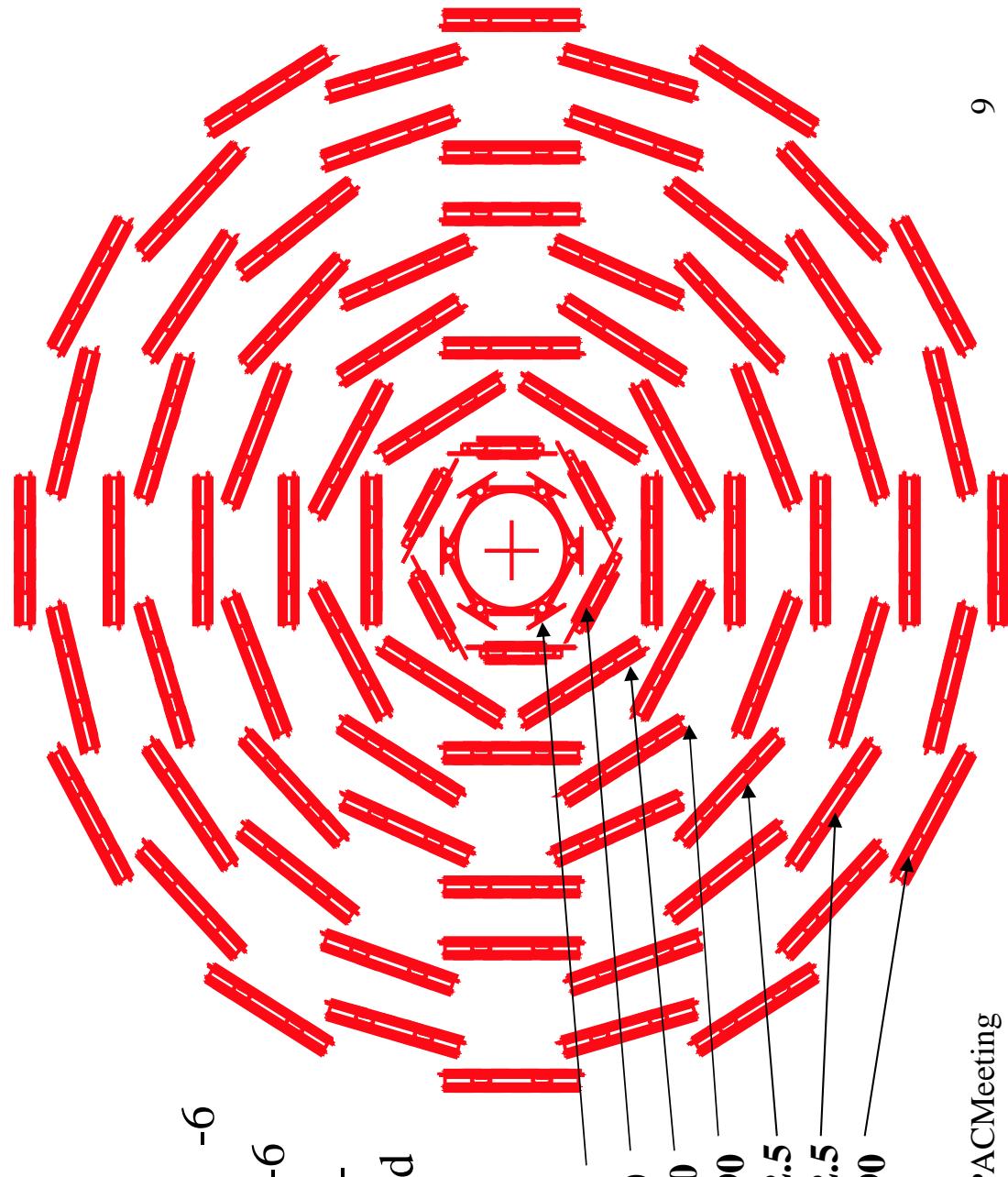
Hybrids and Cables

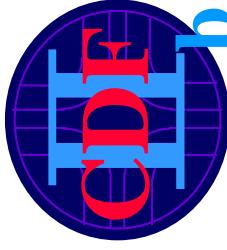
- Hybrids
 - New technology (used on L00) with 50 μm trace/50 μm space and 100 μm via pitch
 - Can now fit a power bus layer and signal traces on a single layer, reducing the total number of layers to 4
 - Result is much smaller hybrid wrt SVXII
- Fine Pitch Signal Cables (L00 style) use only on L0
 - Limit risk of procuring parts and difficult assembly
 - Limit cost – small number of different styles of L00
 - S/N non-negligible when using these cables (\Rightarrow only if strictly necessary)
 - Penalty in mass is minimal ($\sim 0.3\%$ RL) with great benefit in term of assembly, handling, testing, commissioning



RunIIIB Layout

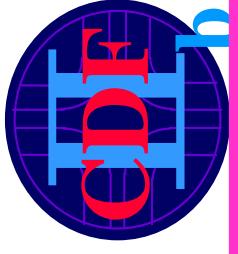
- Ø Doublesidedstaves:
axial and stereosensors
- Ø Uniform design for L2 -6
- Ø L1 very similar to L2 -6
- Ø L0~L00 with only 2 -
chipsensors and supported
by beam -pipe



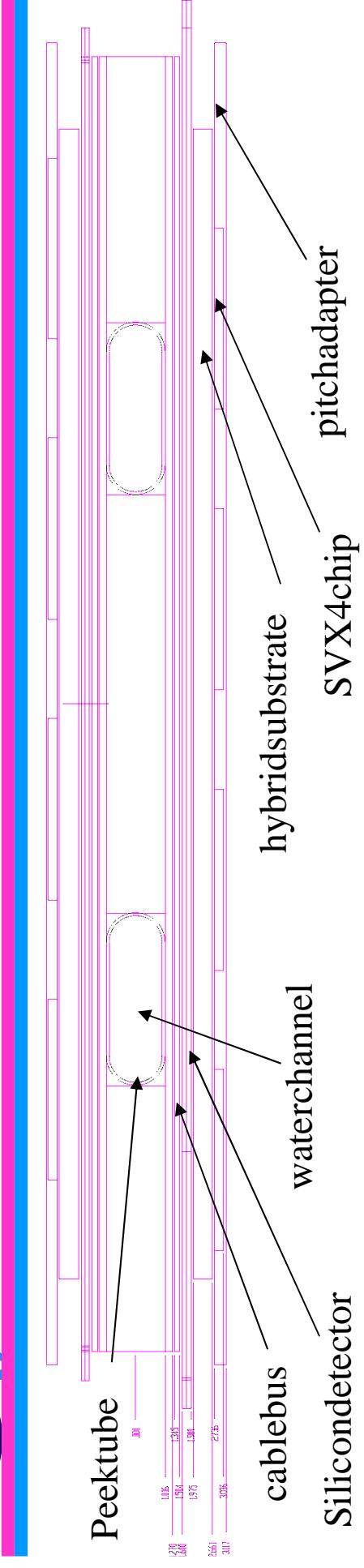


RunIIIB Layout

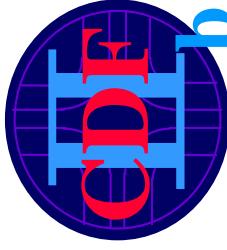
- Uniform stave (ladder) design for ~90% of the detector
 - L2-6 = 156 staves - only one set of fixturing to develop (SVXIII A had 180 ladders, 5 different sizes, 36 of each size)
 - L1 = 12 staves - very similar to L2 - 6
 - L0 ~ L00 type construction
- Small number of different parts
 - Only 4 types of hybrids (SVXIII + L00 had 12 hybrid types)
 - L2-6 have 3 sensor types (SVXIII had 5)
 - L0 and L1 have 2 types of sensors (L00 had 2 types)
- Construction flexibility
 - Can swap layers 2 - 6
 - Flexible descoping
- Further simplification may be possible



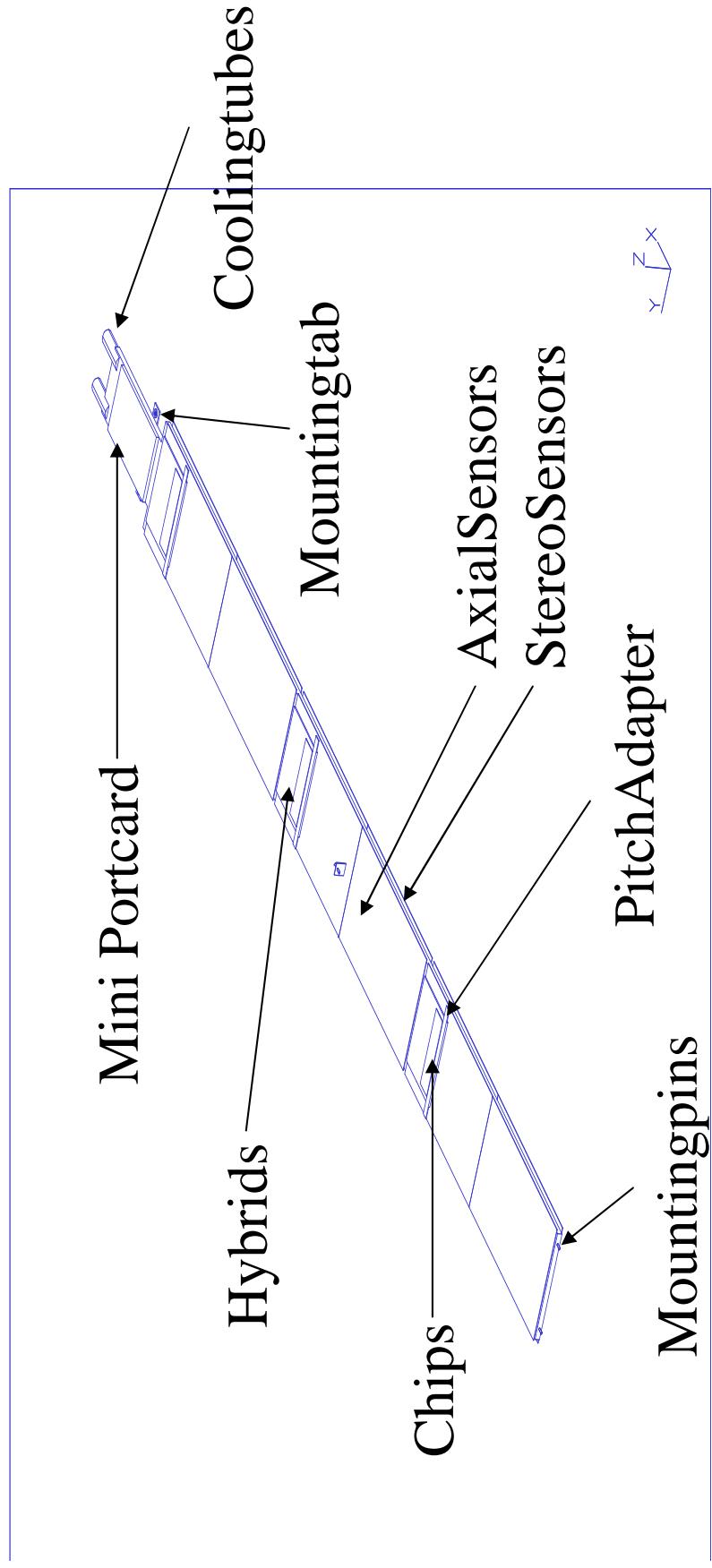
RunIIB Staves

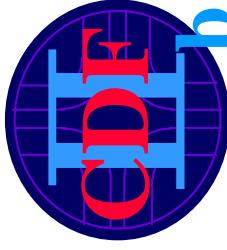


- Stave structure(60cm long, supported at $z=0$ and -60cm):
 - Carbon fiber – rohacell structure with $\sim 2\text{mm}$ peek cooling pipes
 - One each side:
 - 6 single sided silicon sensors
 - 3 hybrids glued to the silicon.
 - Silicon glued to copper – kapton bus cables
 - Hybrids wirebonded to bus cable through gaps between sensors
 - At end of stave mini port card with this bonded to the bus. It regenerates the signals to/from the SVX4 chips.



RunII BStave

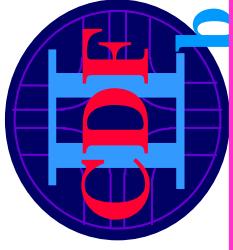




Layout Details

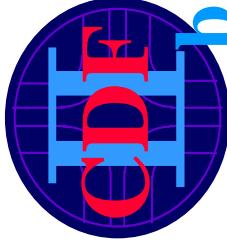
	Layer		Radii (mm)	ϕ segm.	Z segm.	Sens. width	Sens. Leng.	Sens. pitch	n. of Hyb.	Chips per hybrid	Tot. sensors	Tot. Hybrids	Tot. chips
outer	6	A	155.0 \div 166.0	24	6	92.11	47.06	88/44	3	4	288	144	576
	6	90°	151.5 \div 162.5	24	6	92.11	49.0	88/44	3	4	288	144	576
	5	A	125.0 \div 136.0	20	6	92.11	47.06	88/44	3	4	240	120	480
	5	2.5°	121.5 \div 132.5	20	6	92.11	49.0	91.5/45.75	3	4	240	120	480
	4	A	95.0 \div 106.0	16	6	92.11	47.06	88/44	3	4	192	96	384
	4	2.5°	91.5 \div 102.5	16	6	92.11	49.0	91.5/45.75	3	4	192	96	384
	3	A	64.5 \div 77.0	12	6	92.11	47.06	88/44	3	4	144	72	288
	3	90°	61.0 \div 73.5	12	6	92.11	49.0	88/44	3	4	144	72	288
	2	90°	49.0	6	6	92.11	49.0	88/44	3	4	72	36	144
	2	A	45.5	6	6	92.11	47.06	88/44	3	4	72	36	144
inner	1	A	33.5	6	6	74.7	14.8	50/25	3	2	72	36	72
	1	90°	30.0	6	6	74.96	37.0	95/47.5	3	3	72	36	108
	0	A	19.5 \div 23.5	12	6	74.7	14.8	50/25	3	2	144	72	144
TOTAL													
TOTAL (SVXII+L00)													
TOTAL increase (%)													
2,160 1,080 4,068													
864 768 3,276													
250% 40% 24%													

All sensors use alternate stripreadout,
936/1080 hybrids are 4-chippers



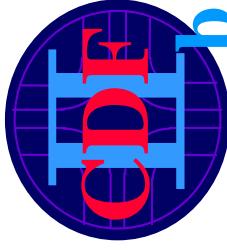
RadiationDamage and Cooling

- Keepsiliconcooltolimittheamountofnoiseincreased due to leakage current and limit thereverseannealingeffect
- Studiesoftheseeffectssettemperaturelimits:for $S/N>10$ for 30fb^{-1}
 - Layers4 -6: $T<15^{\circ}\text{C}$
 - Layers2and3: $T<10^{\circ}\text{C}$
 - Layers0and1: $T<-5^{\circ}\text{C}$
- Requiresactivecoolingofstaves
 - Coolingtubesintegratedintostavestructure
- TotalheatloadverysimilarRunIIA~3KW
- Canuseexistingcoolingsystemwithincreasedglycol concentration(43%)foroperationat -20°C



Stave Material and Stiffness

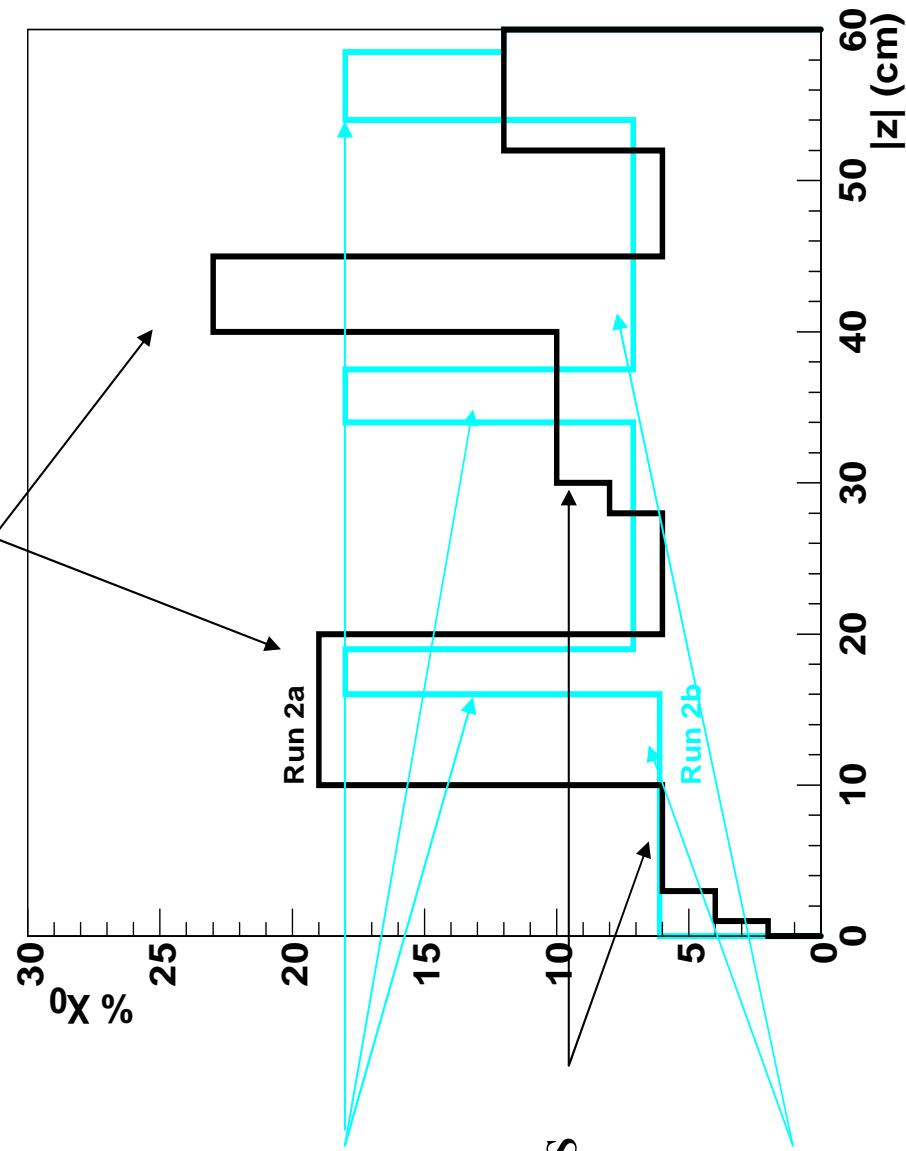
- Stiffness traded for light construction
- Average material over area of stave: $1.5\% \times 0$ per stave:
 - Ø 42% of total silicon sensors (2 sensors 320um thick = 0.64X0)
 - Ø 33% in CF, cooling tubes, water, glue
 - Ø 12% in hybrids
 - Ø 9% in bus cable
- Ø 4% in MiniPC (actually outside tracking region)
 - FEA of structure found that sag was $\sim 170 \mu\text{m}$ over 60cm length
 - Can tolerate up to $\pm 80 \mu\text{m}$ over a module ($\sim 20\text{cm}$ length)
 - No need for midspan support mentioned in TDR
 - Making prototypes to verify FEA results
 - Can reduce sag by increasing thickness of change in mass



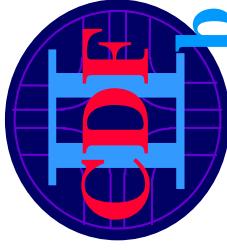
Compare Material in RunIIA with IIB

Material seen by
90deg.tracks

SVXIIIhybrids

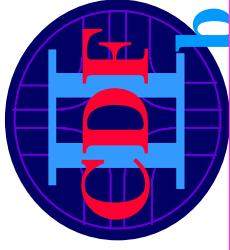


SVXIIIPCandcables
RunIIBstave
structure and bus
cable



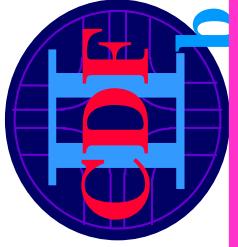
DAQ Changes from RunIIA

- Ø New chip requires changes in frontend of DAQ: New hybrids (smaller!)
- Ø Optical components unavailable and not ready hard:
 - New mini port cards (smaller, minimal active components)
 - New Fiber Transition Modules (No Fibers!, use copper instead)
- Ø New Power Supplies: off-the-shelf, not custom
- Ø No changes upstream of the FMs
- Ø Reduced mass in tracking volume and improved accessibility
- Ø Significant reduction in number of different components
- Ø Number of readout chains fits in existing infrastructure
- Ø SVT can be enhanced to work with RunIIB layout
 - Modifications similar to those made for L00



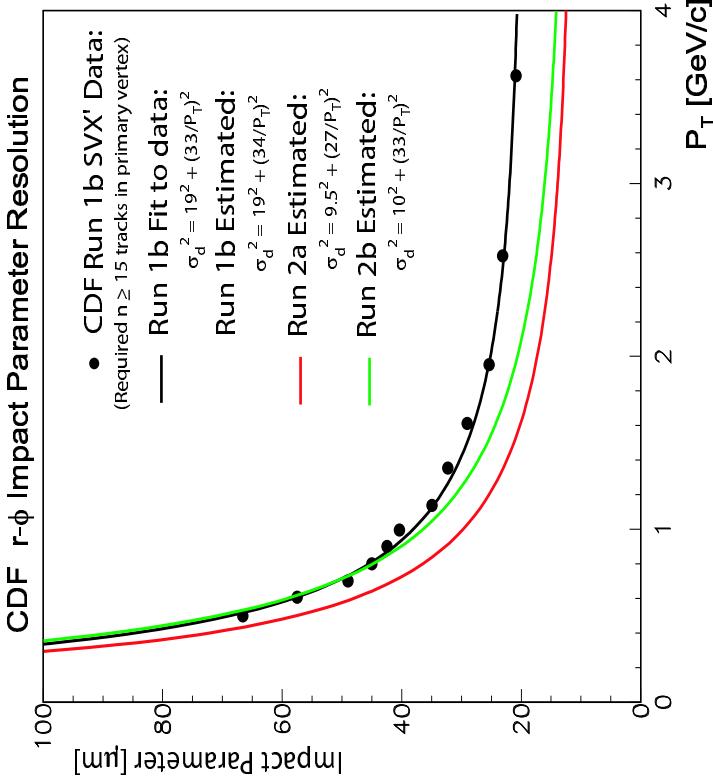
Layout Considerations

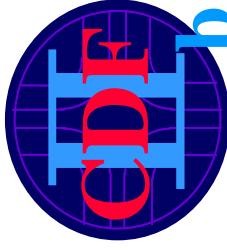
- For the 90deg sensors there are questions about occupancy, hit confusion and wide clusters at large eta.
- Studies in TDR addressed these issues with standalone programs
- Would like to have confirmation with full simulation and data
- Also under consideration is the deterioration of pattern recognition in COT as the inner layers become fully occupied at high luminosity.
- Such considerations may call for more small angle stereolayers.
- We continue to have the 90deg. in the design because of the potential benefit in tagging efficiency (10 - 15% found with 3D tracks over 2D)
- CDF has set up a committee to review the design in light of these global tracking issues
- Standard design is independent of type of sensors (can accommodate axial-90, axial-SA or A-A)
- Decision needed before final order of production sensors (Spring 02)



Resolutioncalculations:Compareto Run1bData

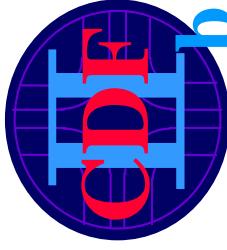
- Analyticprogram
 - Ø Inputhitresolutionsandmaterial
 - Ø CalculateIPorpointingresolution asafunctionoftrackmomentum
- Run1bdatacomparison
 - Ø Calculation: $13 \oplus 34/\text{pt} [\mu\text{m}]$
 - Ø Thenincludeprimaryvertex uncertainty($\pm 10 \mu\text{m}$)andwedgegotowedge misalignments($\pm 10 \mu\text{m}$)
 - Ø **19 \oplus 34/ pt**
 - Ø Measurement: **19 \oplus 33/ pt**
- Verygoodagreement!Canuseto estimateperformanceofRun2A and2BDetectors





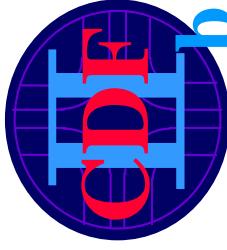
Run2bImpactParametersandPointing

- Goals
 - GoodIPresolutionforhigh efficiencybytagginginRun2b
 - Redundancy: goodIPresolutioniftheinnermostlayeris missed
- Resulting estimated IP resolutions:
 - Axial: $6 \oplus 34/\text{pt}$ and without/innermost $\rightarrow 11 \oplus 66/\text{pt}$
 - Stereo: $8 \oplus 71/\text{pt}$ and without/innermost $\rightarrow 16 \oplus 126/\text{pt}$



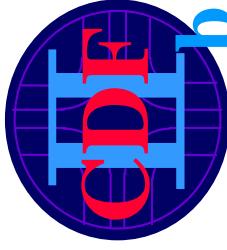
TrackingStudiesw/Run2Offline

- Use Run2a Offline
 - δ Performed Outside -In(OI) axial tracking and Outside -In Stereo(OI2) tracking in COT region a TopMC.
 - Run2a TopMC:
 - > Plot axial and stereo impact parameters
 - > Estimate tracking efficiencies by cutting out tracks who set track parameters are more than σ from generated track parameters
 - > Look at track purity as defined by correct hit usage one each layer
 - Btagging in 2D versus 3D assuming Run2 bIPresolutions
 - > Efficiencies vs E_T and η
 - > Impact parameters of b daughter tracks and prompt tracks relative to both the b decay vertex and the primary vertex

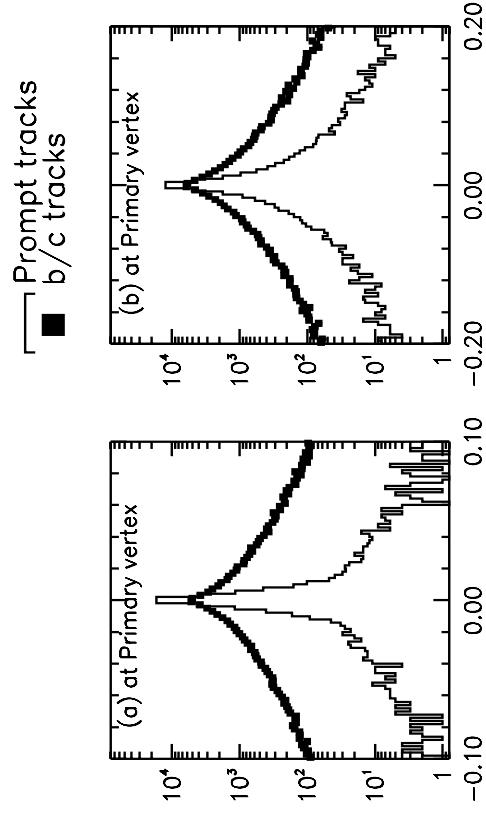


MCBtagging: 2D vs 3D

- Perform a simple version of SECVTX tagging on tracks from MC top jets using smeared generator level info
 - δ Assume 90% track efficiency
 - δ Isolation: Tracks must beat least 240 μm apart at $r=5\text{cm}$
 - δ Resolutions: comparable to those expected in Run 2b
 - Compare tagging for 2D and 3D Impact parameter definitions
 - δ 3D can improve tagging by at most ~10 - 15%
-
- (a)
- ttb(175)
- Tagging efficiency
- Et of bjet (GeV)
- 200
- 150
- 100
- 50
- 0
- 0.0
- 0.4
- 0.8
- 1.2
- (b)
- Tagging efficiency
- Eta of bjet (GeV)
- 2
- 1
- 0
- 1
- 2
- 0.0
- 0.4
- 0.8

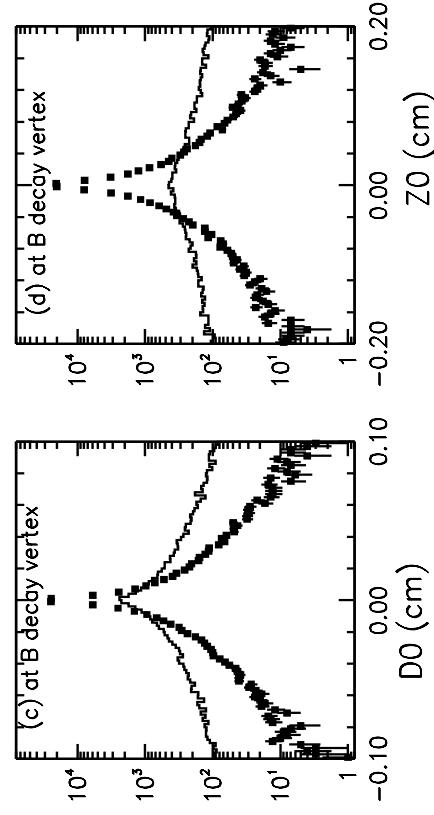


Zmatching

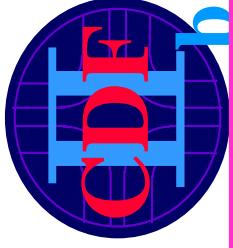


- In2Dallpairsoftracksoverlap
 - Mostbadtracksaredisplaced
- Impact of 3D:tightzmatching requirement can help 2tracktags**

Figure(d) At the B vertex:

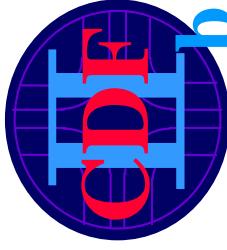


- stereoimpactparameter
distributionismarrowforb
daughtersandbroadforprompt
tracks
- matchingtoafewmm(e.g.w/o
90° info.) provides no help
- At $\sim 100 \mu\text{m}$, (with 90deg.)
additional rejection is possible



Cost and Schedule Strategy

- Build a few functional prototypes this spring, costs include:
 - ❖ prototypes sensors, hybrids, MPC etc. (need to order ASAP)
 - ❖ Develop fixtures for building modules and staves
- Assume chip engineering run is successful enough that another run is not needed
 - ❖ place production order after prototype is shown to work
 - ❖ Can learn enough to order preproduction hybrids
- Preproduction (fix problems with prototypes, hopefully these are final)
 - ❖ Costs include new hybrids, MPC, bus cables
 - ❖ Modify or build a new set of fixtures for modules and staves
- Production costs: components and fixtures to sustain 1 stave/day (1.5 peak)
 - Follow recommendations of PPD Cost review (June 01) for prototype and testing costs, need to determine chip development costs
 - Labo estimate will follow but not yet included in total cost

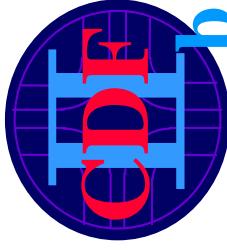


RunIIB Silicon project cost estimate

	Cost	Cost+Cont.
Run2b silicon Project total	\$7,515,300.00	\$9,769,890.00
Sensor Total	\$2,334,000.00	\$3,034,200.00
DAQtotal	\$2,855,300.00	\$3,711,890.00
Construction(Modules and staves)	\$851,000.00	\$1,106,300.00
Beampipe	\$200,000.00	\$260,000.00
Support Mechanics	\$585,000.00	\$760,500.00
Cooling and Interlocks	\$100,000.00	\$130,000.00
Final Assembly	\$190,000.00	\$247,000.00
Mechanical Infrastructure	\$400,000.00	\$520,000.00

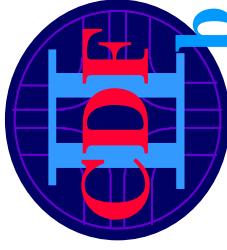
These estimates are still being refined

- Scale of project is about right
- Assume global 30% for contingency



RunIIB Silicon Project Costs

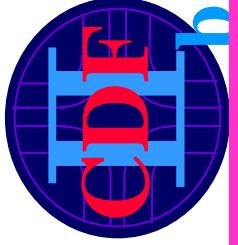
	Sensor Total	\$2,334,000.00
DAQtotal	\$2,855,300.00	
SVX4Chips	\$380,000.00	
Hybrids	\$950,300.00	
BusCables	\$104,500.00	
MiniPortCards	\$441,500.00	
JunctionPortCards	\$62,000.00	
Cables	\$246,000.00	
FTMs	\$101,000.00	
DAQ Testing & Readiness	\$50,000.00	
Power Supply System	\$520,000.00	



Cost and Schedule 2001 - 2002

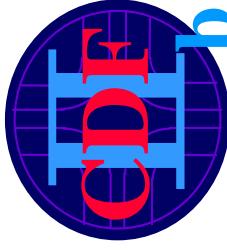
Fall01 to March02	R&D: chip eng.run, sensors, hybrids, L0cables,DAQ(MPC,JPC) Stave mechanics and cooling tests Order beam pipe, CMM for SIdet	Cost total \$1.5M
March02	All parts in hand to build full functioning prototypes/staves	
June02	Order production chips, and sensors Preproduction hybrids	Cost Total \$3M
Fall02	Assembly of preproduction staves with Production chips Order production hybrids, MPC	Cost Total \$2.5M

Rest of project cost (\$0.5M) is spread over 2003 and 2004



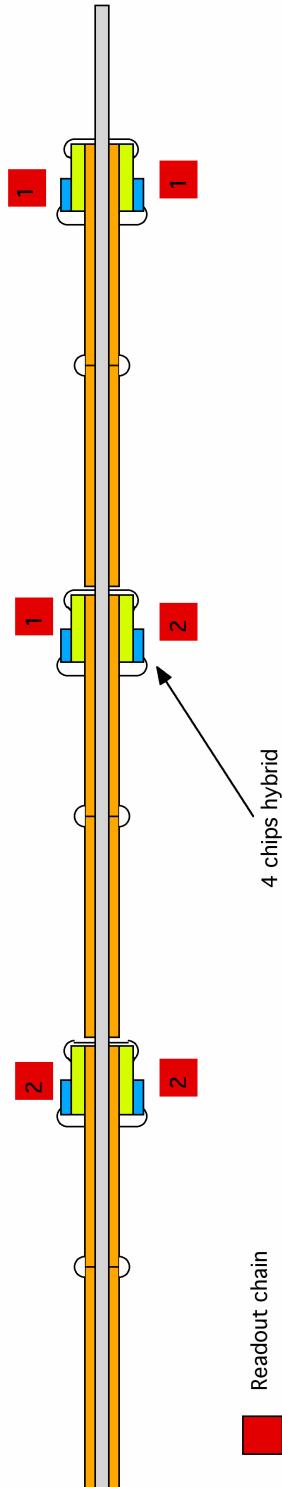
Schedule 2003 - 2005

Jan.03	Production ramp -up 1-2 staves/week
March03	Full production, 1 stave/day
May03	Barrel assembly starts, keeps up with stave production
Dec03	Stave production and barrel assembly finished, final assembly and testing begins
July04	Ready for installation, Shutdown begins
Jan.32005	Silicon installed, collision hall closed

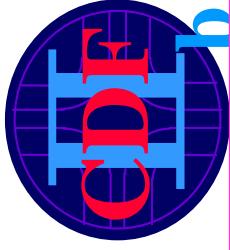


Stave Construction and Testing

Stave Design Concept

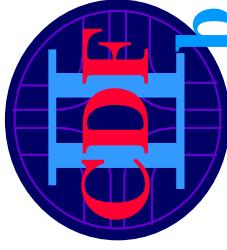


- Modules: Pairs of sensors are first glued head-on, then a 4-chip hybrid is glued onto one end of the silicon.
- Mechanical staves (carbon fiber, rohacell, sandwich with cooling tubes) are assembled separately then a cable is laminated onto both sides.
- Modules and the MPC are glued onto the stave and bonded to the stave through gaps between modules.
- Complete staves are tested and burned in.



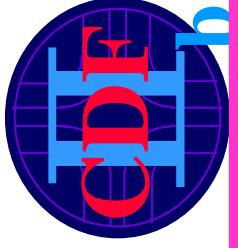
Labor Estimates at peak production

- Technicians - need total of 16(SVXII had 14 at peak)
 - Ø Mech.techs:3(modules)+3.5(staves)+1(barrels)=7.5
 - Ø Wirebonders:2+1 support/setup
 - Ø Testing and repair:1
 - Ø Alignment/inspection:1.5
 - Ø Backup3
- Electricaltechs:2 for assembly of MPC,JPC,cables
- Engineering
 - Ø 3 Mechanical engineers
 - Ø 2 mechanical Design/Drafters
 - Ø 1.5 Electrical engineers (for MiniPC and JPC)
 - Ø 1.0 layout/designer



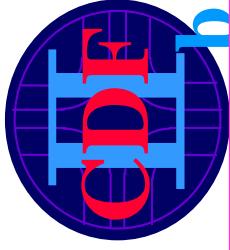
Conclusions

- Highly modular and buildable design for the Run2b Silicon Detector
 - Enhances tracking capability of the present design
 - Total mass in tracking volume is reduced
 - DAQ simplified, active components are more accessible
 - Preparation of detailed Cost and Schedule is in progress
 - Ø Numbers presented represent scope of project
 - Ø Will update estimates with quotations
 - Ø Will include labor
- With appropriate resources and support, we can complete the Run II B silicon project by July 2004 and install it during the 6m shutdown.**



StaveMaterial

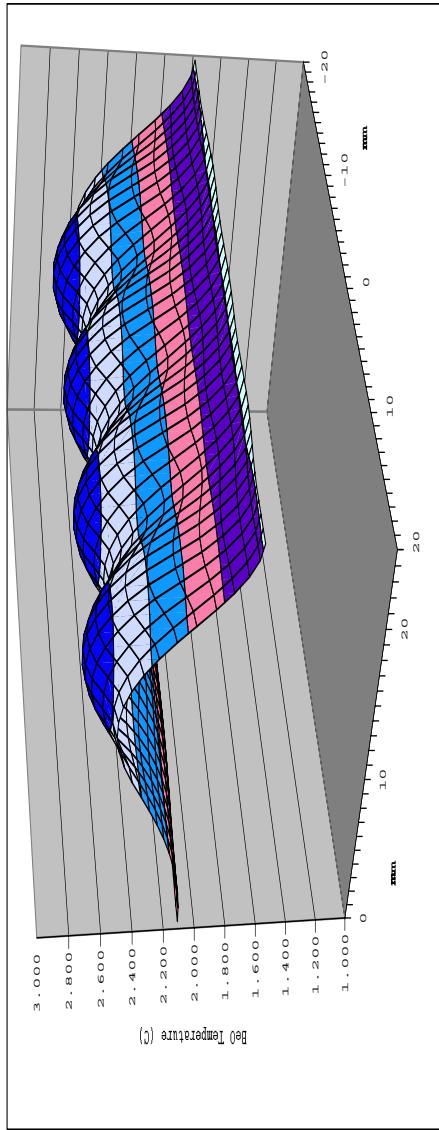
partname	material	X0	length	width	thick	um	factor	scaleT	%X0	%oftotal	subtotal%
detectors	silicon	93.6	92.5	47	0.32	12	1	0.596	0.637	42.335	42.335
carbonfiberfacing	CF	230	561	47	0.25	2	1	0.471	0.205	13.605	
foam	rohacell	13800	561	47	3	1	1	2.824	0.020	1.361	
staveepoxy	epoxy	186	561	47	0.075	2	1	0.141	0.076	5.047	
peektubing	PEEK	319	561	12	0.1	2	1	0.048	0.015	1.002	
watercoolant	water	360	561	12	1.3	2	1	0.625	0.174	11.540	32.555 3i,stave,cool
hybridsubstrate	BeO	144	25	40	0.381	6	1	0.082	0.057	3.768	
dielectric	glass	100	25	40	0.038	18	1	0.024	0.024	1.624	
shieldplane	Au	3.35	25	40	0.008	6	0.47	0.001	0.024	1.598	
goldplanespower	Au	3.35	12	40	0.008	6	0.47	0.000	0.012	0.767	
goldplanesground	Au	3.35	12	40	0.008	6	0.47	0.000	0.012	0.767	
goldtraces	Au	3.35	25	40	0.006	12	0.094	0.000	0.007	0.480	
SvX4chips	silicon	93.6	10	6.8	0.3	24	1	0.017	0.019	1.242	
conductingeponxi	silver*	8.54	10	6.8	0.025	24	0.1	0.000	0.002	0.113	
ceramiccaps0805	dielectric	35	2	1	1.2	12	1	0.001	0.003	0.195	
ceramiccaps1206	dielectric	35	3.2	1.6	1.27	6	1	0.001	0.004	0.265	
ceramiccaps0603	dielectric	35	1.6	0.8	0.9	48	1	0.002	0.006	0.375	
tantalumcaps	tantalum	4	2	1.25	1	6	0.75	0.000	0.010	0.668	
resistors0402	Al2O3	35	1	0.5	0.5	72	1	0.001	0.002	0.122	11.984 hybrids
buskapton	kapton	287	440	40	0.025	4	1	0.063	0.022	1.456	
busCtraces	copper	14.3	440	32	0.017	2	0.81	0.014	0.097	6.436	
busAlplane	aluminum	89	440	35	0.012	2	1	0.013	0.015	0.986	8.878 bus
fanoutsubstrate	Al2O3	75.5	2.75	47	0.375	8	1	0.014	0.018	1.219	
fanouttraces	aluminum	89	2.75	47	0.005	8	0.4	0.000	0.000	0.006	
MiniPCsubstrate	BeO	144	35	40	0.381	1	1	0.019	0.013	0.879	
dielectric	glass	100	25	40	0.038	8	1	0.011	0.011	0.722	
goldplanespower	Au	3.35	25	40	0.008	1	0.47	0.000	0.004	0.266	
goldplanesground	Au	3.35	25	40	0.008	1	0.47	0.000	0.004	0.266	
goldtraces	Au	3.35	25	40	0.006	3	0.2	0.000	0.004	0.255	
XCVRchips	silicon	93.6	2	2	0.5	10	1	0.001	0.001	0.051	
conductingeponxi	silver*	8.54	2	2	0.025	10	0.1	0.000	0.000	0.003	
ceramiccaps0805	dielectric	35	2	1	1.2	20	1	0.002	0.005	0.326	
tantalumcaps	tantalum	4	2	1.25	1	2	0.75	0.000	0.003	0.223	
resistors0402	Al2O3	35	1	0.5	0.5	20	1	0.000	0.001	0.034	4.249 mini-PC
										1.504	
											total



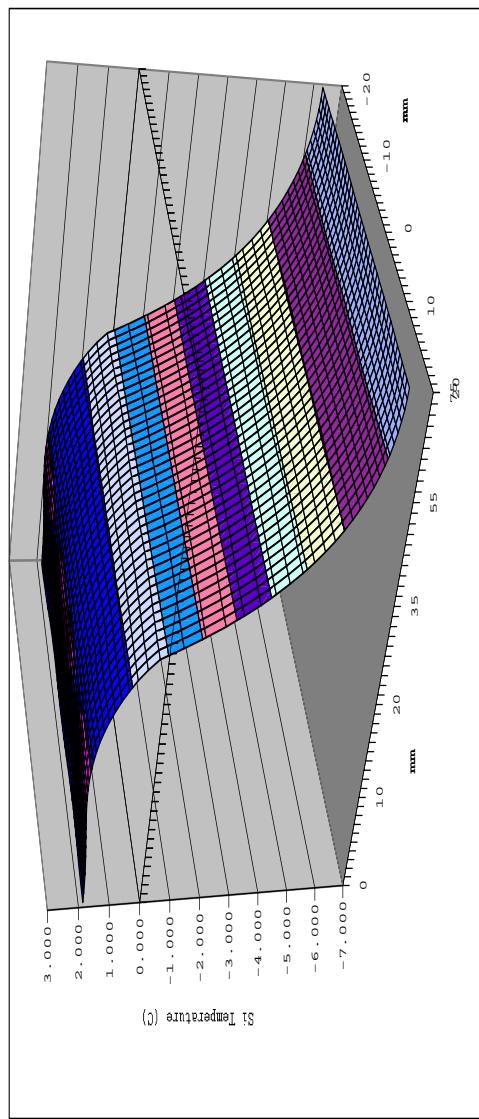
CoolingStudies

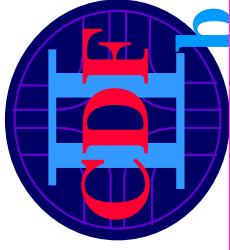
- Model:
 - Ø 4-chip hybrid over one sensor
 - Ø Hybrid is 15 mil BeO, 25 mm long
 - Ø Silicon is 0.3x75
 - Ø Bus cable is 0.214 thick with 0.18 W/m -K
 - Ø Core skin is 3 plies Carbon fiber
 - Ø Cooling tube is speck 0.1 mm thick and 5 mm flat area
 - Ø Coolant T = -9C
 - Ø Convection to 10C gas

Base Case Hybrid Temperatures



Base Case Silicon Temperatures





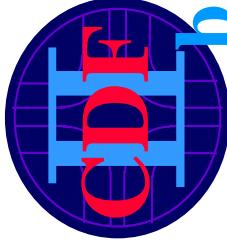
Cost comparison to June estimates

	JuneCost\$	JuneCont.k\$	%cont.	junetotal	2-Nov	+30%cont	Nov2/junetot	Nov2/junebase
Sensors	1130	283	0.25	1413	2334	3034.2	1.65	2.07
chips	196	98	0.50	294	380	494	1.29	1.94
2-chip hybrids	208	42	0.20	250	125	162.5	0.50	0.60
4chip hybrids	727	145	0.20	872	825.3	1072.89	0.95	1.14
minipc	54	19	0.35	73	441.5	573.95	6.05	8.18
hdsets(bus+mpc=pc)	70	35	0.50	105	239.5	311.35	2.28	3.42
JPC	43	15	0.35	58	62	80.6	1.07	1.44
FTM+cables	200	70	0.35	270	212	275.6	0.79	1.06
Misc. adapt/test	50	20	0.40	70	50	65	0.71	1.00
powersupplies	400	267	0.67	667	520	676	0.78	1.30
powercables	20	10	0.50	30	0	0	0.00	0.00
beampipe	200	100	0.50	300	200	260	0.67	1.00
Mech/cool	1000	500	0.50	1500	1626	2113.8	1.08	1.63
signalcables	489	366	0.75	855	100	130	0.12	0.20
elec. Test/burnin	100	50	0.50	150	0	0	0.00	0.00
Misc. extras	0	0	0	0	400	520		
total	4887	2,020	0.41	6907	7515	9769.89	1.09	1.54

- Very different design (June was all like L00 design)

- June estimate was for production – R&D was considered to be before project was baselined, most prototyping was in contingency
- PPD Cost Review recommendation: put prototyping in base cost
- New estimate also includes equipment upgrades for SiDet
- June cost + contingency very close to Nov -2 total

Brenna Flaugh Nov.2,011 PAC Meeting



Cost comparison to AprilPAC

- Can also go back to April estimate, but that was based largely on guesses

	AprilCostk\$	Aprilcontk\$	AprilTalkk\$	JuneCostk\$	JuneCont.k\$	%cont.	JuneTotal	June/April	v0.5	v0.5/junet	v0.5/junebase
Sensors	1038	519	1557	1130	283	0.25	1413	0.91	2334	1.65	2.07
chips	222	111	333	196	98	0.50	294	0.88	380	1.29	1.94
2-chip hybrids	317	166	483	208	42	0.20	250	0.52	125	0.50	0.60
4chip hybrids	427	220	647	727	145	0.20	872	1.35	825.3	0.95	1.14
minipc	98	49	147	54	19	0.35	73	0.50	441.5	6.05	8.18
hdsets(bus+mpc=jpc)	111	56	167	70	35	0.50	105	0.63	239.5	2.28	3.42
JPC	20	10	30	43	15	0.35	58	1.93	62	1.07	1.44
FTM4-cables	91	45	136	200	70	0.35	270	1.99	212	0.79	1.06
Misc.adapt/test	0	0	0	50	20	0.40	70		50	0.71	1.00
powersupplies	300	200	500	400	267	0.67	667	1.33	520	0.78	1.30
powercables	0	0	0	20	10	0.50	30		0	0.00	0.00
beampipe	200	100	300	200	100	0.50	300	1.00	200	0.67	1.00
Mech/cool	600	400	1000	1000	500	0.50	1500	1.50	1626	1.08	1.63
signalcables	360	252	612	489	366	0.75	855	1.40	100	0.12	0.20
elec.Test/burnin	0	0	0	100	50	0.50	150		0	0.00	0.00
Misc.extras	0	0	0	0	0		0		400		
total	3784	2128	5912	4887	2,020	0.41	6907	1.17	7515	1.09	1.54